# Dopant-Independent and Voltage-Selectable Silicon-Nanowire-CMOS Technology for Reconfigurable Logic Applications

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***Abstract*— In this paper, we report on the fabrication and characterization of a novel voltage-selectable (VS) nanowire (NW) CMOS technology suitable to extend the flexibility in circuit design and reconfigurable logic applications. Silicon NW-structures with Schottky-S/D-junctions on silicon-on-insulator (SOI) substrate are used to realize dopant-independent unipolar CMOS-like transistors. A selection of the device type (PMOS or NMOS) is performed by application of an appropriate back-gate bias. The versatile programming capability of this approach is demonstrated in a VS-NW-CMOS inverter set-up.**

## I. INTRODUCTION

Silicon nanowires (Si-NW) are intensively investigated by many research groups and considered as promising replacement for standard MOSFET based transistor technology, since classic geometric downscaling of planar MOSFET devices is reported to come to an end [1]. However, the ambipolar [2] nature of the nanowires turns out to be a roadblock, as p-type and n-type transistors are basic building blocks for today's complementary MOS logic, i.e. its simplest device, the inverter [3]. Concerning bottom-up NW-fabrication, a vapour-liquid-solid growth approach is often not compatible with standard CMOS technology, in view of the used catalyst materials, as well as the need of high growth temperatures during the fabrication process. Other unsolved problems occur during doping [4,5] (e.g. dopant segregation), thus the use of grown nanowires in large-scale integration of integrated circuits is not very likely. As we will show, most of these issues could be circumvented by the top-down fabrication of unipolar Si-NW devices with Schottky contacts for source and drain. Furthermore, our approach is based on controlling the transistor-type (i.e. NMOS or PMOS) of the device via the back-gate voltage, leading the way for switchable transistor characteristic changeable on the fly. Furthermore, when the transistor type, i.e. NMOS or PMOS, could be simply defined by programming via applying a bias, additional flexibility of reconfigurable logic circuit design is expected [6] for programmable logic (FPGA, CPLD) and system-on-chip (SoC) applications. For means of fabrication, a standard top-down technology was used, forming the nanowire by well-known lithography and subsequent reactive ion etching. Fig. 1. gives a schematic view of the device set-up on a MultiSOI substrate [7].

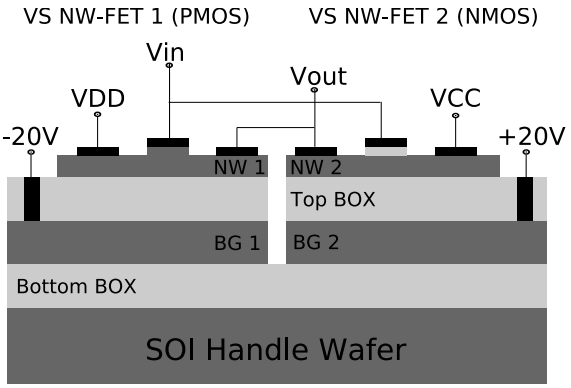


Figure 1. Schematic of realized inverter on multi-SOI substrate. The transistor type (NMOS or PMOS) is selectable by the application of an appropriate back gate bias to the corresponding back-gates, i.e. BG1 and BG2, respectively.

## II. FABRICATION

The devices are fabricated on ultrathin-body SOI substrates from SOITEC with a top-silicon thickness of 70 nm, a buried oxide thickness of 145 nm and a boron doping level of $10^{15}$ $cm^{-3}$. The substrates are prepared with alignment marks for the subsequent electron beam lithography (EBL). By means of EBL, a 90 nm wide line is defined into the negative resist, and transferred onto the top-Si layer via reactive ion etching in hydrogen bromide (HBr) plasma. In the following the substrate is oxidized in a horizontal furnace at

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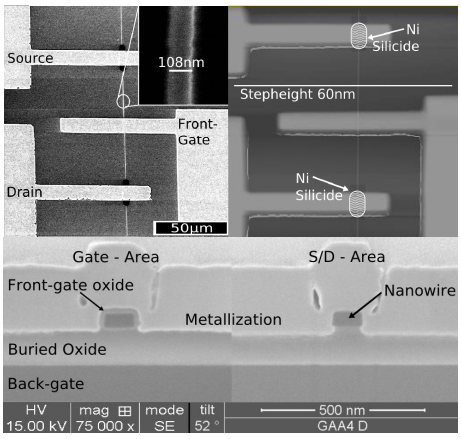


Figure 2 top left: SEM image of the fabricated devices. The nanowire width is measured as 108nm, gate length is 5µm. Top right: AFM scan of the device, the channel height is 60nm, only areas directly beneath source and drain contacts are salicided. Bottom left: Cross-sectional SEM (XSEM) image of the gate area. Note the top tri-gate structure (i.e. front-gate). The gate oxide thickness amounts to 9nm. Bottom right: XSEM of the source/drain region with Schottky S/D strucure.

1000°C for 7 minutes, forming the gate oxide of 9 nm for the tri-gate nanowire device. Subsequently contact holes for S/D contacts are formed via EBL and wet chemical etching in hydro-fluoric acid (HF). Contact pad lithography is also performed by EBL using a dual-layer resist system based on poly methyl methacrylate (PMMA) and novoresist [8] especially developed for EBL lift-off purposes. Metallization of S/D contacts and gate electrode is realized by electron beam evaporation of 70 nm nickel with a 180 nm aluminum capping on top. Subsequently the S/D contacts are silicided at 500°C for 10 minutes in a tube furnace. During this forming gas treatment a mixture of 90% nitrogen and 10% hydrogen is used, where the nickel reacts with the silicon surface forming a mid-gap NiSi-Schottky-barrier contact [9] to the low doped silicon nanowire. Fig. 2 (top) shows several results of process characterization techniques that were used to determine the devices vertical and lateral dimensions. Cross section SEM (XSEM) is used to illustrate the gate area with its tri-gate structure and the S/D area where the salicidation occurrs. From Fig. 2 a channel width of 90nm is determined by subtraction of the gate oxide thickness. The nanowire height is measured to 60 nm with atomic force microscopy (AFM), and the gate to S/D distance corresponds to 20µm Finally, single dies of the SOI-wafer were used to build a voltage-programmable CMOS inverter in a stacked hybrid SOI technology related to the schematic illustrated in Fig. 1.

## III. RESULTS AND DISCUSSION

All the properties of the NW-MOSFET structure are determined through the field-effect via front-gate (FG) and back-gate (BG) voltages as shown in Fig. 3. Similar to the conventional MOSFET, the current transport and hence the switching characteristics, is well controlled through front-gate due to the thin oxide and the tri-gate electrode geometry. However, the back-gate bias determines the transistor type, PMOS or NMOS. For example, when applying a sufficiently large negative voltage to the back-gate the thin top-silicon layer will be depleted of electrons and the accumulation of

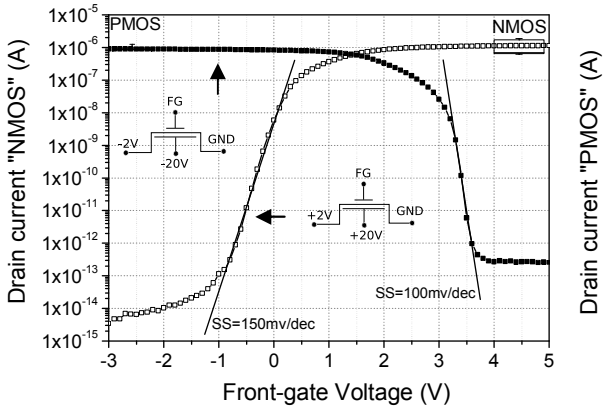


Figure 3. Subthreshold characteristics of voltage-programmable NW-FETs for fixed positive and negative back-gate bias, respectively. Unipolar transistor characteristics are achieved with high on/off current ratios for both, PMOS-type and NMOS-type NW-FETs. Box-plots of on-currents are included to illustrate the impact of process variations.

holes (here: majority carriers) occurs. The resulting transfer characteristics obtained through a front-gate sweep results in a PMOS-like device characteristic. Otherwise applying a positive BG-voltage, the Si-NW will be depleted of holes and eventually, at a sufficiently large BG-bias an inversion layer of electrons forms. The resulting transfer characteristics obtained through a FG-sweep leads to an NMOS-like device characteristic. Fig. 4. emphasizes on the dependence of the drain current from the back-gate bias, whereas a back-gate swing is performed under floating front-gate conditions. It is clearly found, that the corresponding back-gate bias is able to manipulate the devices charge-carrier type. In the transfer characteristic ON/OFF current ratios up to $10^6$ are obtained for both, n- and p-type NW-FETs. However, the PMOS-like NW-FET exhibits the better subthreshold slope of $S_p \approx 100$mV/dec but a higher off-current. The higher off-current results from the slight p-type doping of the initial substrate, the degraded subthreshold slope of the NMOS-like NW-FET is due to the narrow inversion layer not completely extending the 60nm thick silicon wire and related series resistances at the S/D

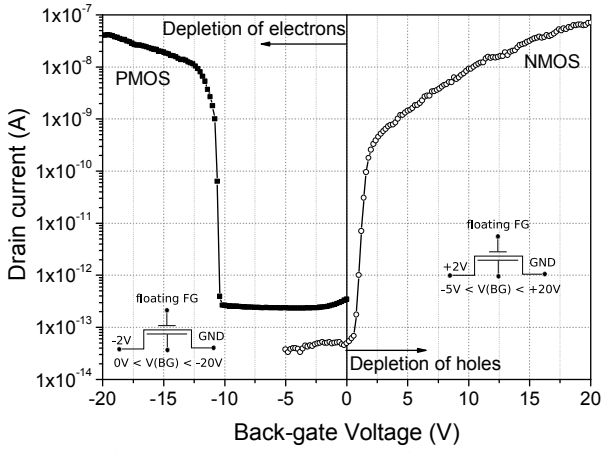


Figure 4. Effect of back-gate bias on NW device properties: Drain current ID measurements as a function of back-gate voltage from -20V < VBG < +20V confirm the change of device types, PMOS vs. NMOS. The front-gate is left floating and a drain bias of -2V (PMOS) and +2V (NMOS) is used, respectively.

contacts. Nevertheless it is obvious that either n- and p-type behavior of the wire can be selected by the applied back-gate voltage.

Based on these results, a VS-CMOS inverter circuit was set up using two arbitrary nanowire devices. The required PMOS and NMOS transistors were defined by voltage-programming via the back-gates, applying a voltage of -20V (PMOS) and +20V (NMOS), respectively. The transfer characteristic of the realized inverter is presented in Fig. 5. Here, a symmetrical supply voltage of ±2V was provided to the inverter to obtain a HIGH/LOW transition near an input-voltage ($V_{in}$) of 0V. As can be seen from Fig. 5, a clean inverter characteristic is achieved with a transition from HIGH to LOW state at $V_{in}$ of 0,25V. As expected for a regular CMOS inverter, both NW-devices are momentarily in the ON-state during transition, resulting in a characteristic short current pulse (open symbols in Fig. 5). However, no significant current is drawn from the power supply when the VS-CMOS NW inverter is in its stable HIGH or LOW state.

The versatility of our programmable CMOS-logic is demonstrated in Fig. 6 which shows two traces of the transfer characteristic of a VS-NW-CMOS inverter. The first input-voltage sweep (solid squares in Fig. 6) is performed when using NW-FET 1 as PMOS transistor and NW-FET 2 as NMOS. In this case the HIGH/LOW transition occurs at a $V_{IN}$ of approximately –1.3 V. For the second sweep (open squares in Fig. 6) the supply and back-gate voltages are reversed, so that NW-FET 1 serves as NMOS transistor and NW-FET 2 as PMOS. Again, a CMOS inverter transfer characteristics is observed, however the transition point is shifted by ± 0.5 V. This shift is due to the fact that the drive currents of the devices do not exactly match, since process-variations during fabrication are very likely in this early stage of technology (cf. box-plots in Fig. 3). Nevertheless, a proof of concept of the voltage-programmed CMOS inverter could be demonstrated.

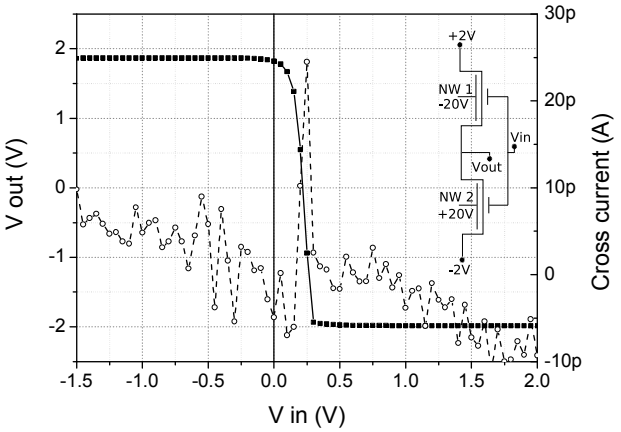


Figure 5. Switching characteristics (solid symbols) of a CMOS inverter circuit formed by CMOS nanowire-FETs via applying the appropriate voltages at the back-gates (see schematic inset). A clear inverter behavior is obtained including the characteristic cross-current peak (open symbols) directly at the HIGH/LOW transition point.

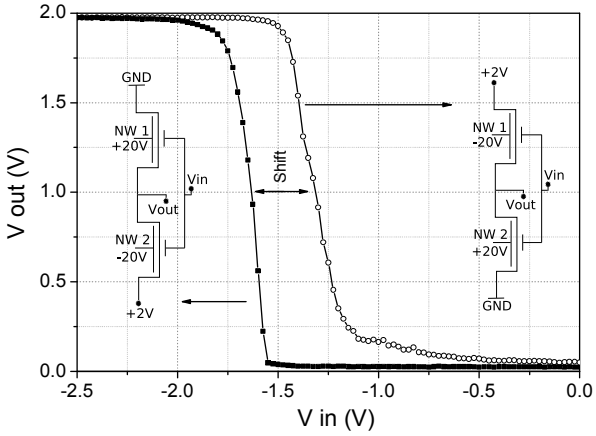


Figure 6. Two traces of the switching characteristics of the VS-NW-CMOS inverter illustrate the versatile programming capability of the VS-NW devices. Filled symbols represent NW-FET1 working as PMOS and NW-FET 2 as NMOS. Interchanging back-gate bias and supply voltage polarity, the transistor types are swapped and again a CMOS-inverter characteristic (open symbols) is observed.

## IV. Conclusion

In conclusion, we have successfully fabricated unipolar NW-FETs on SOI in which the device type (n- or p-type) is selectable by applying an appropriate back-gate bias. These voltage-programmable nanowire FETs exhibit high on/off ratios and can be used in a universal fashion to extend the flexibility in circuit design of reconfigurable logic. The versatile programming capability of this approach was demonstrated experimentally using a VS-NW-CMOS inverter circuit set-up.

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